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RN-6227

B. E. II (Sem. III) (IC) Examination

May / June – 2010

Digital Circuits

Time : **3** Hours] [Total Marks : **100**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ **B. E. 2 (Sem. 3) (IC)**

Name of the Subject :

☛ **Digital Circuits**

☛ Subject Code No. : **6 2 2 7** ☛ Section No. (1, 2,.....) : **1&2**

Seat No. :

Student's Signature

(2) Answers to the **two** sections must be tied **separately**.
(3) Assume suitable data wherever necessary.
(4) Figures to the right indicate full marks.
(5) Attempt all questions.
(6) Question 4 is compulsory.
(7) All symbols carry usual notations.

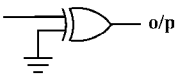
SECTION - I

1 Answer the following questions : **20**

(i) Dual of A(B+C) = _____. **1**

(ii) (A'+B'+C') is equal to _____. **1**

(iii) 1's complement of (101010101) = _____. **1**

(iv) The output of the logic gate 

is _____. **1**

(v) Boolean expression for XNOR is _____ in POS form. **1**

(vi) Explain DeMorgan theorems for three variables. **2**

(vii) Show that AB'C + B + BD' + ABD' + A'C = B+C. **3**

(viii) Reduce following Boolean functions **4**

(a) A'B'C + (A'+B+C')' + A'B'C'D

(b) (A+A') (AB + ABC')

(ix) Write first 10 decimal digits in base 5. **3**

(x) The sum of all minterms of a Boolean function of n variable is 1. Prove the above statement for n=3 variables. **3**

2 (a) Explain full adder with help of circuit diagram and truth table. 7

(b) Implement the function with 8 to 1 multiplexer. Take B, C and D as select variables. 8

$$f(A, B, C, D) = \sum m(0, 1, 3, 4, 8, 9, 15)$$

OR

2 (a) Design a combinational circuit that converts a digits from 8,4,–2,–1 code to BCD. 8

(b) Design a combinational circuit with four input lines that represent a decimal digit in BCD and four output lines that generates the 9's complement of the input digits. 7

3 Attempt any three : 15

(i) Explain the design of 3 bit even parity generator

(ii) Construct a 5 × 32 decoder with four 3 × 8 decoder and 2 × 4 decoder.

(iii) Design 2 bit multiplier circuit.

(iv) Explain 2 bit magnitude comparator.

(v) Explain 8 × 3 encoder circuit.

SECTION - II

4 (a) Answer the following question in brief : 10

(i) State application of flip/flop.

(ii) Compare combinational and sequential circuits.

(iii) State conditions for Race-Ground.

(iv) How many numbers of flipflops are required to build a binary counter that counts from 0 to 1023?

(v) State types of shift register.

(b) Write and explain steps of conversion of flipflop with an example. 10

5 (a) Design a type T counter that goes through states 0.3, 5,6,0. 8

(b) Explain 4 bit ring counter with circuit diagram and wave forms. 8

OR

(b) Explain triggering of flipflops with waveform. 8

6 Attempt any **two** : 14

(a) Explain JK flipflop with preset and clear input.

(b) Explain programmable logic array (PLA) in detail.

(c) Explain serial in serial out shift register in detail.